

NOV 08 2004
U.S. PATENT & TRADEMARK OFFICE
O I P E

PDNO: 10001414-1
Inventor: Scott Ferguson et al
Title: System & Method for Configuring
A Logic Analyzer to Trigger on Data
Communications Packets & Protocols
Page 2 of 10

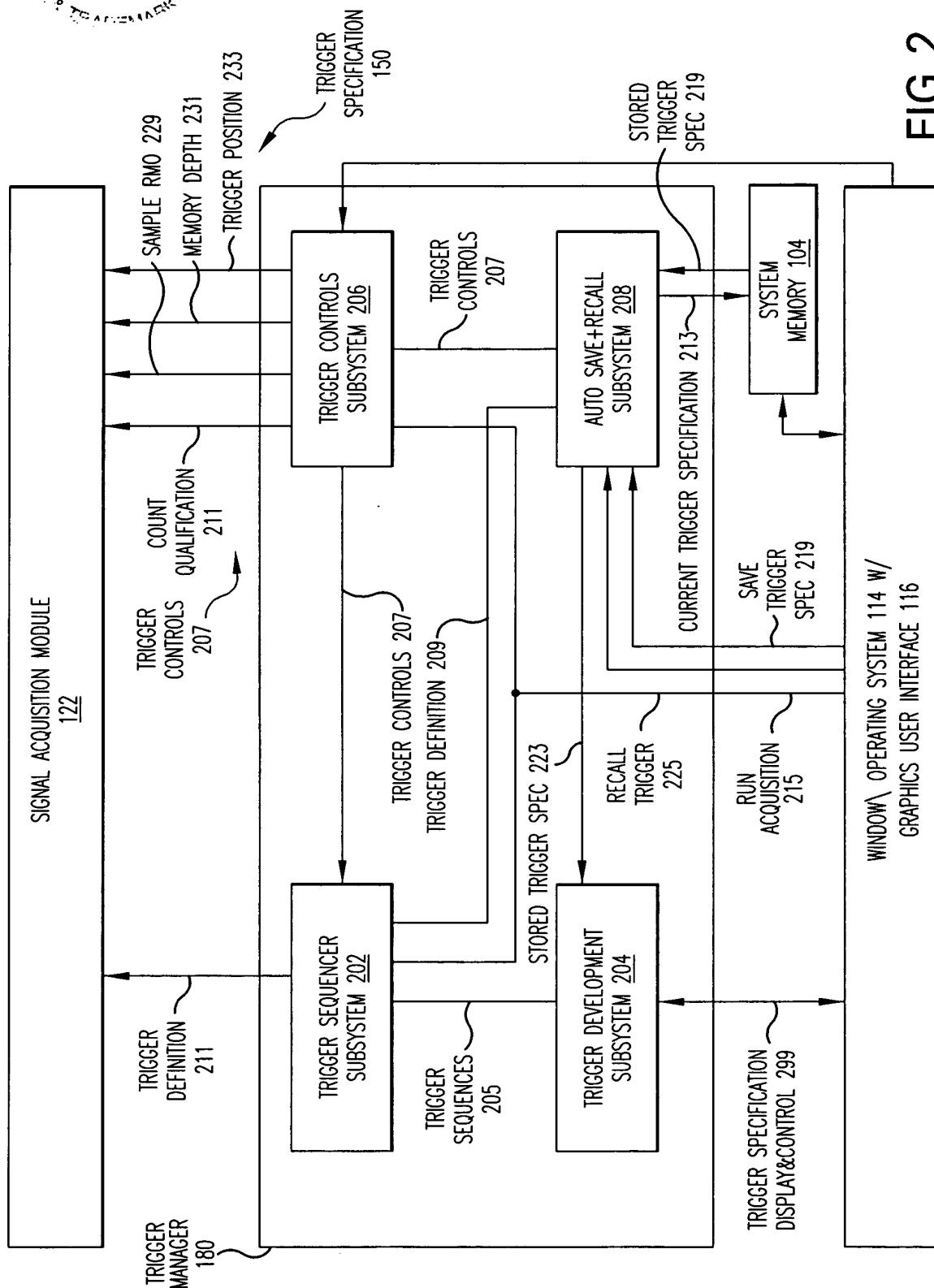


FIG. 2

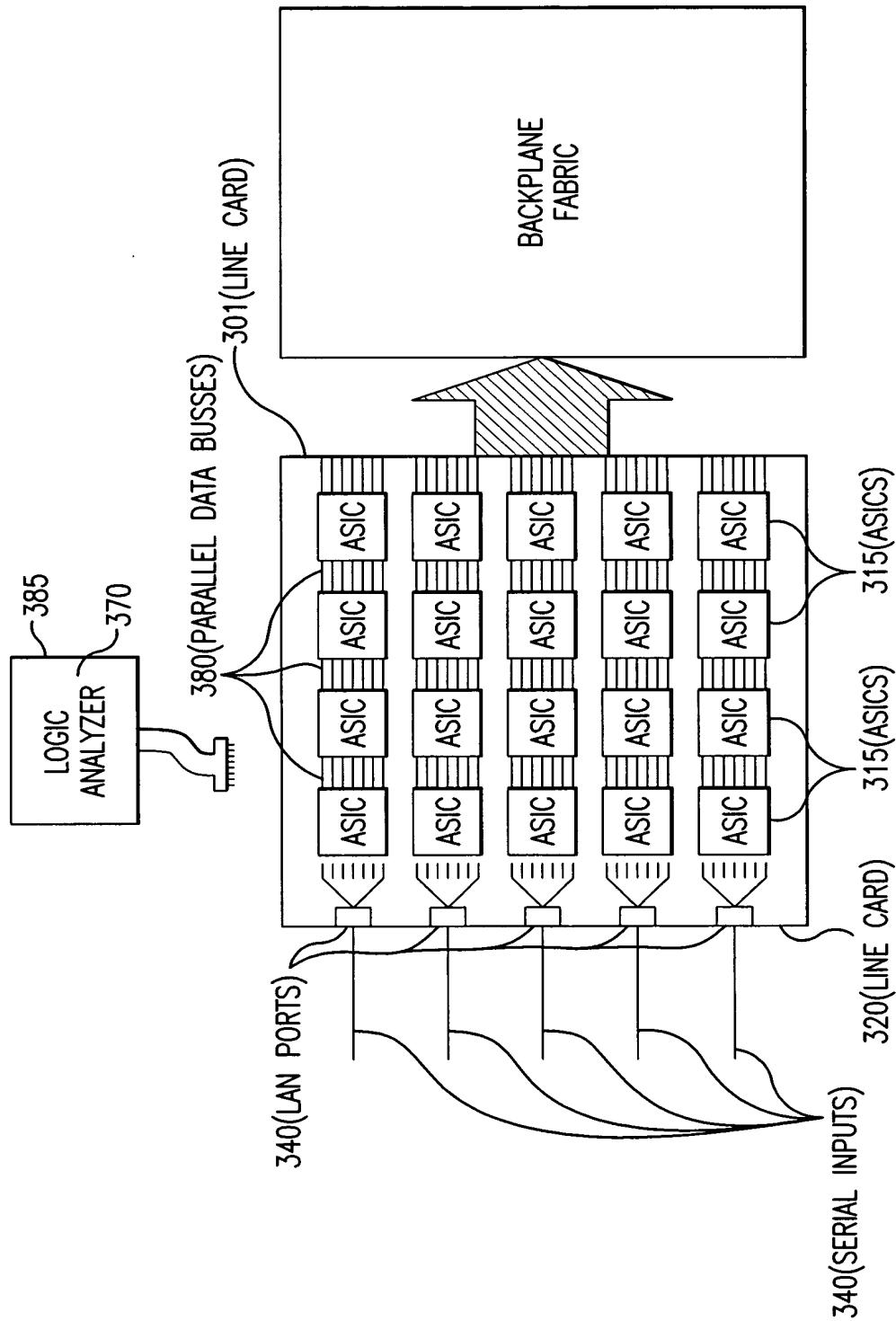


FIG. 3



PDNO: 10001414-1
Inventor: Scott Ferguson et al
Title: System & Method for Configuring
A Logic Analyzer to Trigger on Data
Communications Packets & Protocols
Page 4 of 10

DESTINATION ADDRESS: 48BITS: 1 1-XX-XX-1 1-XX-XX-XX
SOURCE ADDRESS: 48BITS: XX-XX-XX-XX-XX-XX-XX
LENGTH/TYPE: 16BITS: XXXX

FIG.4a

FIG.4b



PDNO: 10001414-1
Inventor: Scott Ferguson et al
Title: System & Method for Configuring
A Logic Analyzer to Trigger on Data
Communications Packets & Protocols
Page 5 of 10

DESTINATION ADDRESS: 48BITS: XX-XX-XX-1 1-XX XX XX
SOURCE ADDRESS: 48BITS: XX-XX-XX-XX-XX-XX-XX-XX
LENGTH/TYPE: 16BITS: 0800

FIG.4c

<u>DATA BIT BLOCK</u>	<u>DON'T CARE MASK</u>
11	00
00	ff
00	ff
11	00
00	ff
08	00
00	00

FIG.4d

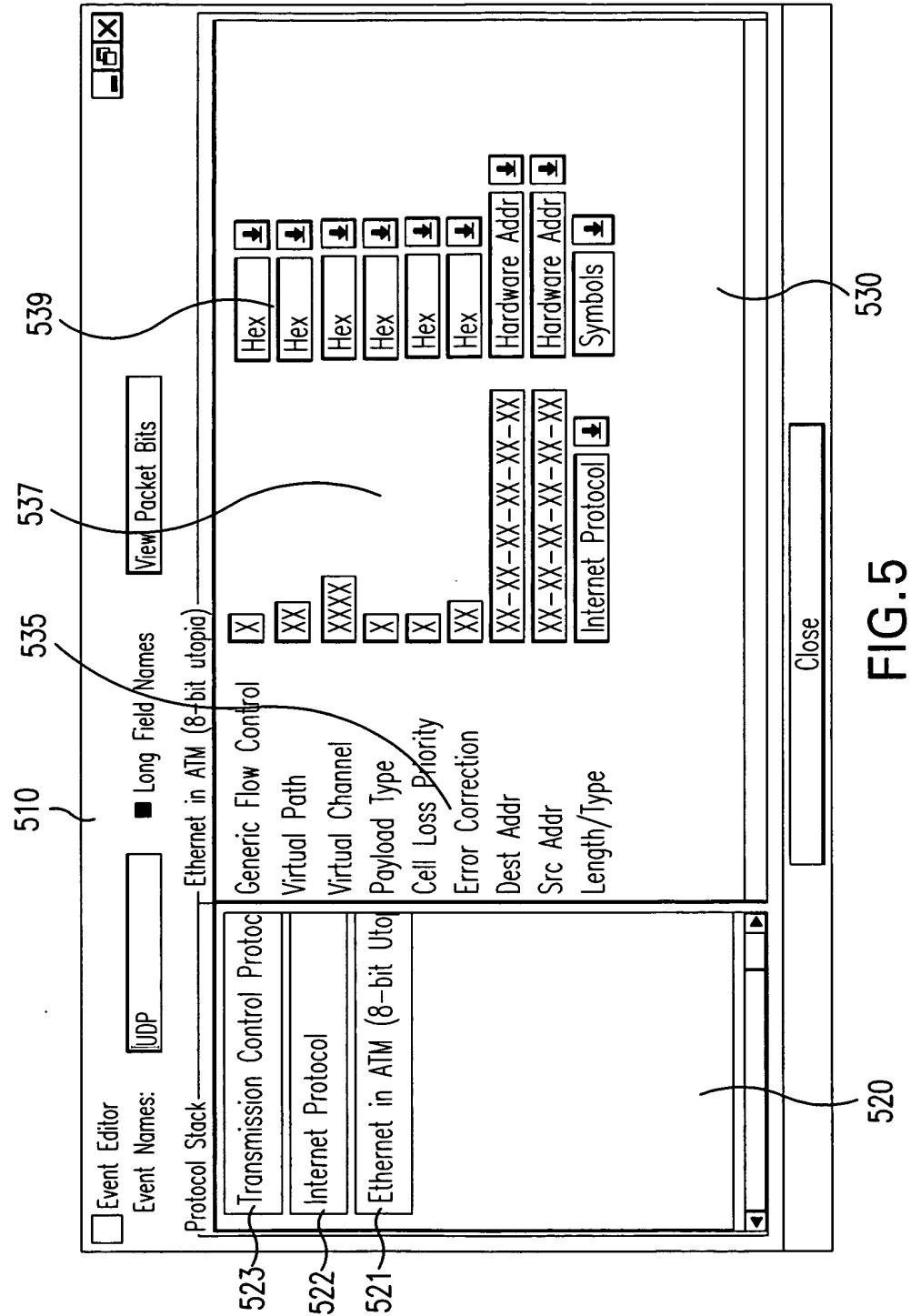


FIG.5

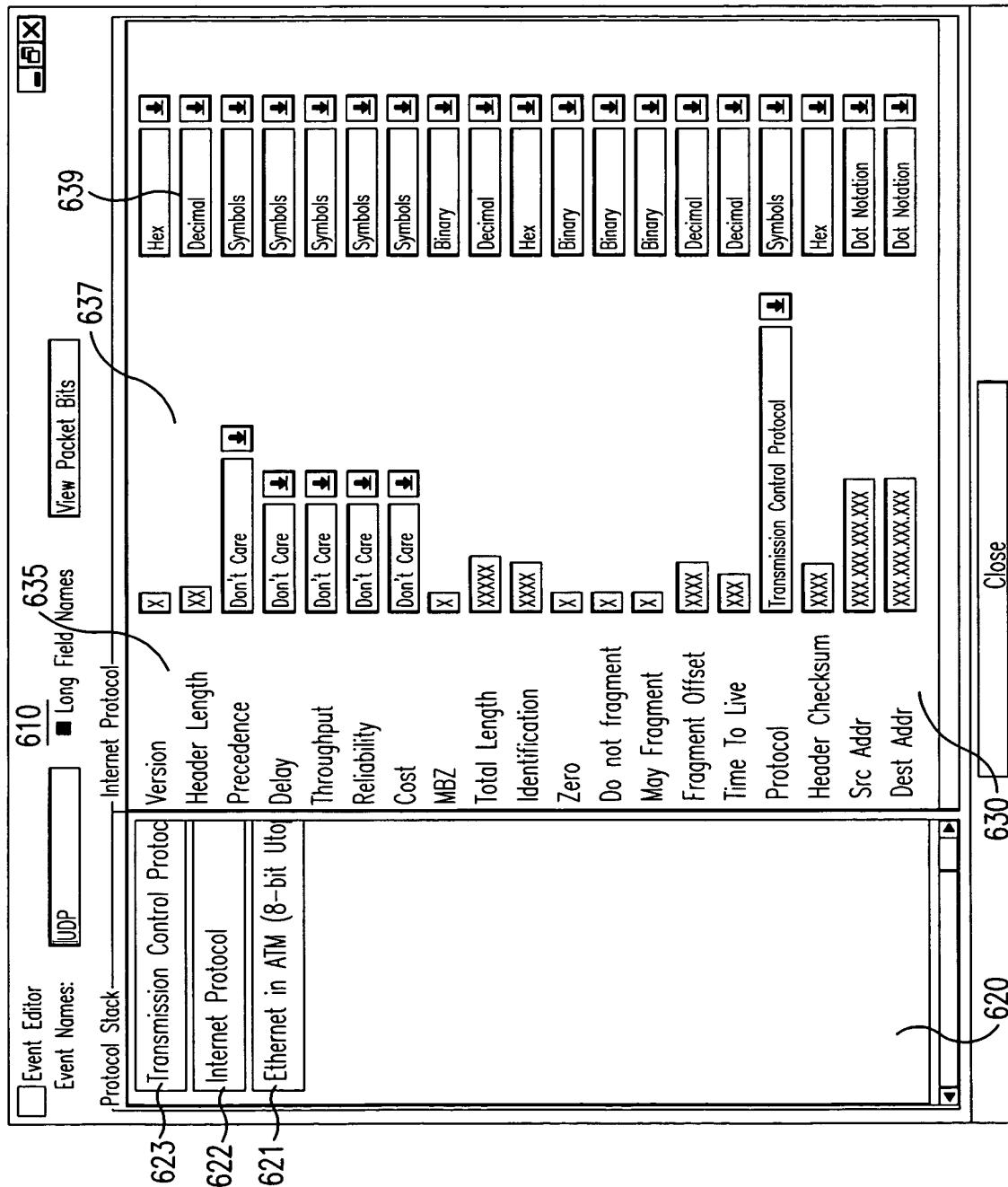
520



PDNO: 10001414-1
Inventor: Scott Ferguson et al
Title: System & Method for Configuring
A Logic Analyzer to Trigger on Data
Communications Packets & Protocols

Page 7 of 10

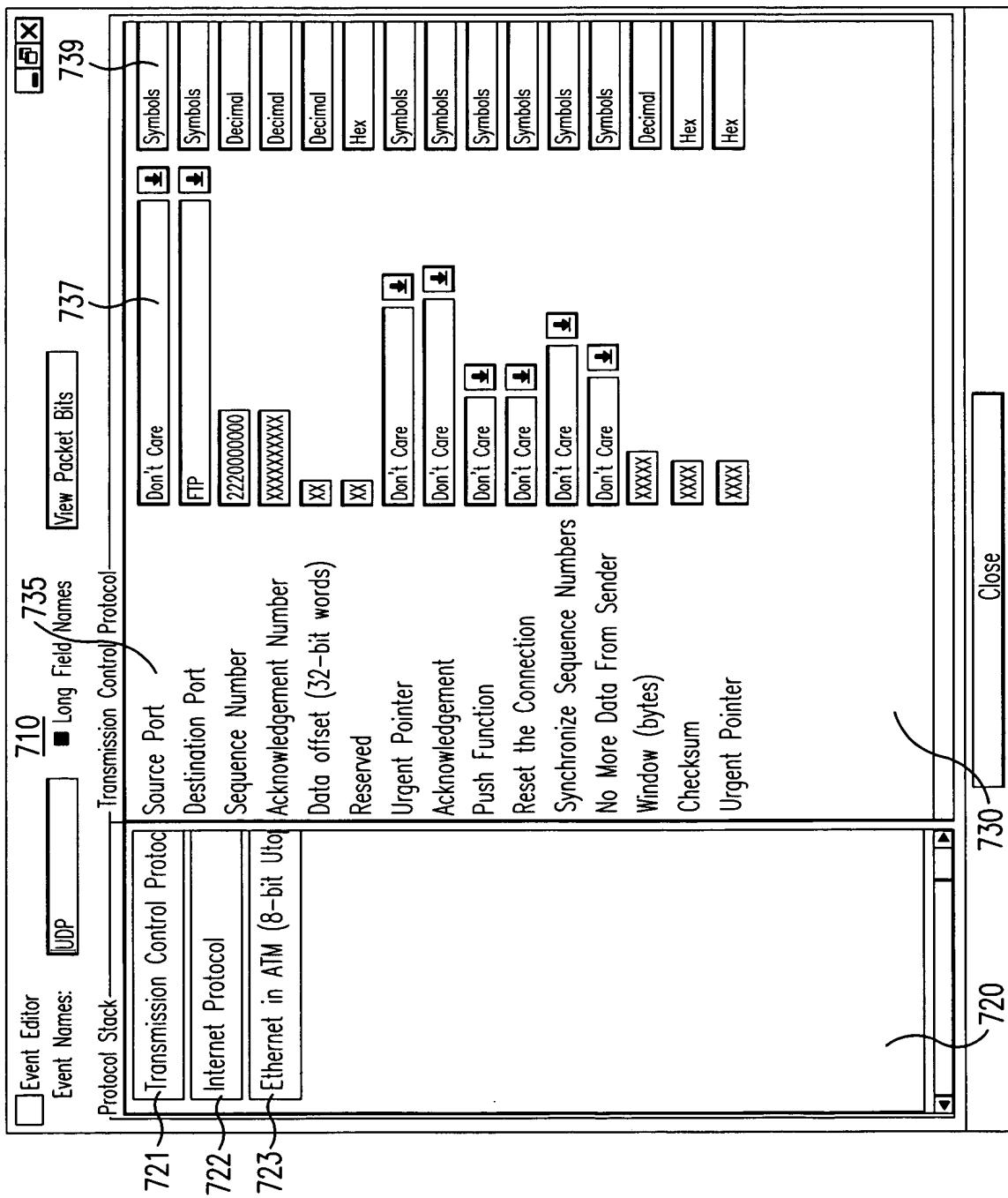
FIG. 6





PDNO: 10001414-1
Inventor: Scott Ferguson et al
Title: System & Method for Configuring
A Logic Analyzer to Trigger on Data
Communications Packets & Protocols
Page 8 of 10

FIG. 7



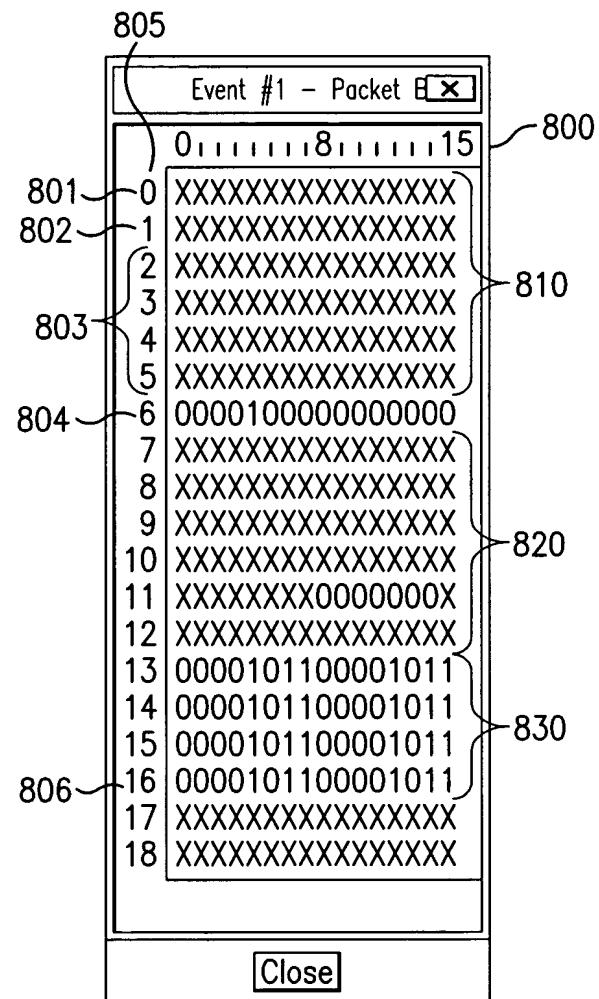
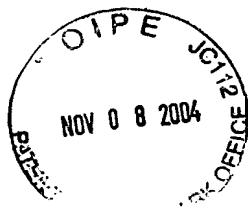


FIG.8a

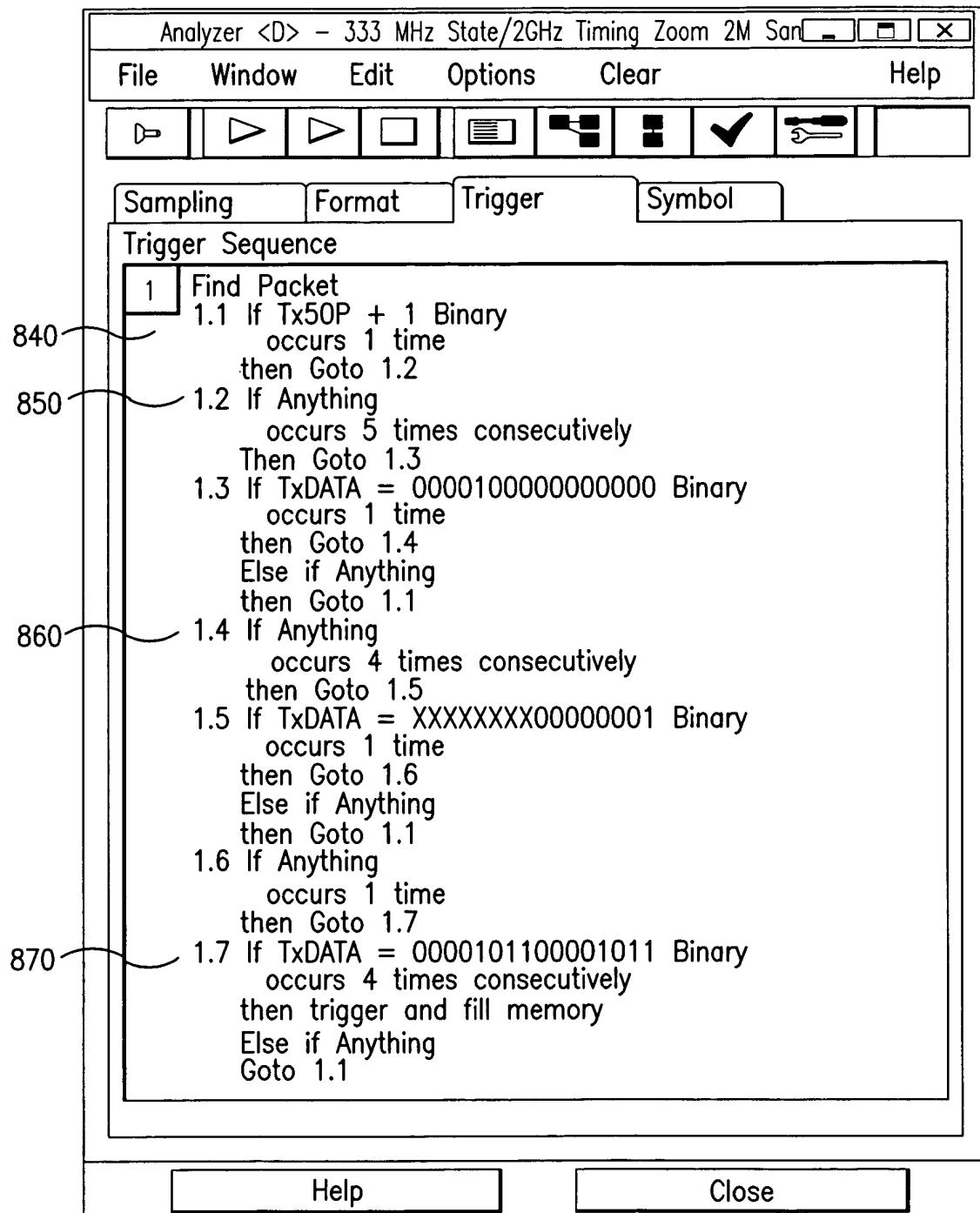


FIG.8b